PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-299421
(43)Date of publication of application : 12.11.1993

(51)Int.Cl. H01L 21/321

(21)Application number : 04-098382
(22)Date of filing : 20.04.1992

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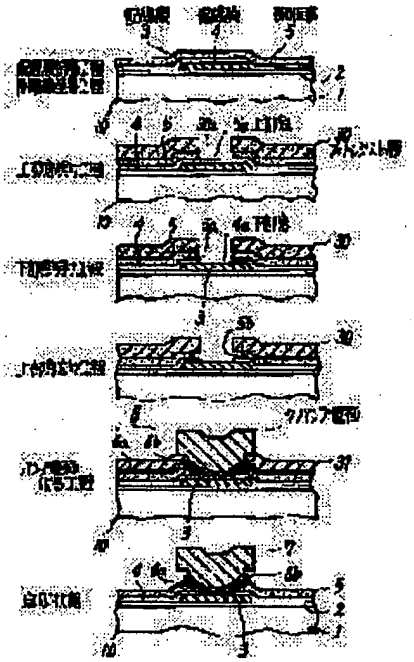
(54) MANUFACTURE OF BUMP ELECTRODE FOR INTEGRATED CIRCUIT DEVICE

(57)Abstract:
PURPOSE: To form a bump electrode on a flip chip of an integrate circuit device with its protective film pr tected by a resin film in a simple process with a high yield.
CONSTITUTION: A protective film 4 is deposited on a wiring film 3 where a bump electrode 7 is to be formed, and then a resin film 5 is applied thereto. A window determining a bump electrode pattern is formed in a photoresist film 30, and further an upper window 5a is formed in the resin film 5 using a dedicated developer. A lower window 4a is formed in the protective film 4 by etching using the resin film 5 as mask. Metal for the bump electrode 7 is grown on a base film 6 connected to the wiring layer 3 exposed in the lower window 4a by electroplating.



LEGAL STATUS

[Date of request for examination]	20.02.1998
[Date of sending the examiner's decision of rejection]	
[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]	
[Date of final disposal for application]	
[Patent number]	3077372
[Date of registration]	16.06.2000
[Number of appeal against examiner's decision of rejection]	
[Date of requesting appeal against examiner's decision of rejection]	
[Date of extinction of right]	

CLAIMS

[Claim(s)]

[Claim 1] How to make the bump electrode which is characterized by providing the following and which was connected to the wiring film at the integrated circuit device. The process which puts a protective coat on a wiring film. The process which applies a meltable resin film with a developer before hardening on a protective coat. The process which ends an up aperture on a resin film with the developer for them at the same time it breaks the aperture which specifies a bump electrode pattern to be the photoresist film applied on the resin film. The process which ends a lower aperture in a protective coat by etching which uses this resin film as a mask, and the process which grows up the metal of a bump electrode alternatively with electrolysis plating on the wiring film exposed into the lower aperture.

[Claim 2] The manufacture method of the bump electrode for integrated circuit devices characterized by using a polyimide resin film for a resin film in a method according to claim 1.

[Claim 3] The manufacture method of the bump electrode for integrated circuit devices characterized by giving the growth process of a bump electrode after passing through the process which extends an up aperture to the side following a lower aperture dawn process in the method

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Industrial Application] this invention relates to the method of making the bump electrode which is a salient electrode for external connection to the flip chip of the integrated circuit device for chip mounting.

[0002]

[Description of the Prior Art] Since an above-mentioned flip chip equipped with the bump electrode for external connection has the feature that chip mounting is carried out in a form as it is, and the space and time and effort of mounting can be saved sharply, without containing in a package, although it is in the inclination increasingly adopted as the inclusion to various electronic instruments widely recently When a heat cycle etc. starts while in use and defects, such as a crack, occur in the protective coat of the front face of a chip, there is a problem which is easy to cause the fall of a property by the invasion of the open air. Hereafter, with reference to drawing 2 , the situation of this defective generating is explained briefly.

[0003] Drawing 2 is the important section enlarged section of a flip chip 20, and the wiring film 3 of aluminum is arranged on the insulator layers 2, such as a wrap silicon oxide, in the front face of the semiconductor substrate 1 where the integrated circuit was made. It is gold so that an aperture may be broken in the wrap protective coat 4 and this wiring film 3 may be connected with the wiring film 3 in it in the chip periphery section on the left-hand side of drawing. Copper The bump electrodes 7, such as solder, protrude with electrolysis plating through the thin ground film 6. The ground film 6 is considered as the two-layer composition of bottom ground film 6a, such as titanium used as a plating electrode like usually at the time of electrolysis plating, and top ground film 6b, such as conductive good PARAJUUMU. In addition, in the case of mounting, the bump electrode 7 is joined with thermocompression bonding or soldering with the other party with the posture which turned the flip chip 20 downward at drawing and reverse.

[0004] In the center section on the right-hand side of drawing, the wiring film 3 is mutually wired in this example through an insulator layer 2 two-layer, and is covered by the protective coat 4. Airtight inorganic high insulating materials, such as a silicon nitride, are used for this protective coat 4, while membraneous quality is precise, when it is hard and tension is applied, there is a weak fault, as shown in drawing, thermal stress may concentrate on the part where a covering level difference is big, and Crack C may occur. If this defect occurs, it is there to the open air. There is a possibility of especially moisture invading, and being easy to make the aluminum of the wiring film 3 corroding, invading also into the semiconductor substrate 1 further, and reducing the operating characteristic of an integrated circuit.

[0005] For this reason, in the flip chip which requires high-reliability, the inorganic protective coat 4 is protected from the former by the film of the quality of organic. To this organic protective coat, it is tough, and heat-resistant good polyimide resin etc. is used. The conventional method which makes the bump electrode 7 in the case of equipping drawing 3 with this resin film is shown. It is this drawing (a) first. This drawing after breaking aperture 4a in a protective coat 4 like (b) The spin coat of the polyimide resin etc. is carried out to the resin films 5 like. After making it fully harden at the temperature of 300 - 400 ** It is this drawing (c) to this. Aperture 5a is broken by the dry etching method etc. like, and it is this drawing

(d) in Apertures 4a and 5a. The bump electrode 7 is grown up with electrolysis plating through the above-mentioned two-layer ground film 6 like. In addition, this drawing (b) The spin coat of the polyimide resin which has photosensitivity as a resin film 5 at a process is carried out, and it is this drawing (c). It can also be made to harden after breaking aperture 5a according to the photograph process at a process.

[0006]

[Problem(s) to be Solved by the Invention] Although the invasion of the open air can be prevented with the resin film 5 and the reliability of a flip chip 20 can be sharply raised even if defects, such as a crack, occur in a protective coat 4 by piling up the resin film 5 of the quality of organic on the inorganic protective coat 4 as mentioned above, time and effort is taken too much as the resin film 5 was added, and also a problem newly occurs along with it. That is, since a photograph process is needed also for the resin film 5 besides the conventional protective coat 4, the part becomes cost quantity. Furthermore, drawing 3 (b) It is following drawing 3 (c) about the resin film 5 which adhered to the wiring film 3 at the process. If it may take completely, it may not go out at a process and contamination by the residue of the resin film 5 or it is shown in the aluminum front face, the faulty connection of the bump electrode 7 will occur and the manufacture yield will fall. The purpose of this invention is to offer the manufacture method of the bump electrode which can solve this cost quantity and problem of a yield fall by addition of a resin film.

[0007]

[Means for Solving the Problem] After putting a protective coat first on the wiring film which should protrude a bump electrode according to this invention method, the above-mentioned purpose applies a meltable resin film with a developer, before hardening on it. An up aperture is broken on a resin film with the developer for them at the same time it breaks the specification aperture of a bump electrode pattern on the photoresist film applied on this resin film. Subsequently, a lower aperture is broken in a protective coat by etching which uses a resin film as a mask, and it is attained by growing up the metal of a bump electrode alternatively with electrolysis plating in the same way as the former on the wiring film exposed into the lower aperture.

[0008] It is good to use polyimide resin for a resin film also by this invention method, especially the thing of an ammonia system is advantageous and, as for the developer for the dissolution, it is good organic alkalinity and to use a positive form for a photoresist film corresponding to this. In order to form in the longitudinal section of the configuration of an upper breadth advantageous to it the aperture for bump electrodes which consists of a lower aperture and an up aperture, it is desirable to give the process which extends the up aperture of a resin film to the side with a developer following on the lower aperture dawn process of a protective coat before the growth process of a bump electrode. In addition, as for the heat hardening of a resin film, it is good to carry out in advance of the growth process of a bump electrode.

[0009]

[Function] By this invention method's applying a resin film, before ending the aperture for bump electrodes in a wrap protective coat in a wiring film unlike the former, and using a meltable thing with a developer, before hardening to this By breaking an up aperture on a resin film with the developer for them at the same time it breaks the aperture which specifies a bump electrode pattern to be a photoresist film, and breaking a lower aperture by etching which makes it a mask to a protective coat As the need of adding a photograph process like before for a resin film is abolished, and the number of processes is decreased and a resin film does not contact a wiring film through all processes, generating of the faulty connection of the bump electrode by the contamination etc. and a wiring film is prevented.

[0010]

[Example] The example of this invention is explained with reference to drawing 1 . For a bump electrode, the state for every main processes which are made by the wafer before isolating to each flip chip, and constitute this invention method is this drawing (a). - (f) It is shown by the important section enlarged section of a wafer 10, and the same sign as the portion corresponding to drawing 2 or subsequent ones is attached. Drawing 1 (a) The front face of the semiconductor substrate 1 where the integrated circuit of BAUEHA 10 was made so that it might be shown is by the insulator layer 2 of a silicon oxide or phosphorus silicate glass. The wiring film 3 of aluminum with a thickness of about 1 micrometer which was covered by 0.5-1-micrometer thickness, and was connected with the integrated circuit in parts other than illustration at the bottom is arranged.

[0011] Drawing 1 (a) The state where the protective coat covering process and the resin film covering process were ended is shown. At a protective coat covering process, the protective coats 4, such as a silicon nitride, are put

1-micrometer thickness by the plasma CVD method etc. like usually all over the wafer 10 including the wiring film 3 top. It is drawing 3 (a) at this stage conventionally. Although the aperture was broken in the protective coat 4 like, by this invention method, the resin film 5 is succeedingly applied on it at the following resin film covering process, without breaking an aperture. It is good and the spin coat of the resin liquid diluted with the solvent to proper viscosity is carried out all over a wafer 10 by 2-3-micrometer thickness, and at the resin film application process of a parenthesis, having tough intensity after hardening on this resin film 5, and using polyimide resin with high thermal resistance evaporates only a solvent, it follows by un-hardening, and stops and puts on a state meltable to a developer.

[0012] Drawing 1 (b) An up aperture dawn process is shown. At this process, after carrying out the spin coat of the photoresist film 30 all over the wafer 10 first and printing the pattern of the bump electrode which are usually a diameter of dozens of micrometers, and an angle in a photograph process on this, the resin film 5 is dissolved with the same developer, and up aperture 5a is broken at the same time it extracts aperture 30a to it with a developer. In the developer for these simultaneous aperture dawns, it is the organic alkali of an ammonia system. (for example, AZ303) Using is good and it is good to use a positive form for the photoresist film 30 corresponding to this.

[0013] Drawing 1 (c) A lower aperture dawn process is shown. At this process, lower aperture 4a is broken in a protective coat 4 by etching which uses the resin film 5 equipped with up aperture 5a as a mask, and the aluminum of the wiring film 3 is exposed. 5 - 10% of O2 is included in this aperture dawn etching like usually. Although it is possible to use the dry etching which makes CF4 reactant gas, it is desirable to give over etching and to fully defecate the front face of the wiring film 3 until lower aperture 4a of a protective coat 4 becomes large a little from up aperture 5a of the resin film 5 in this case. In addition, since the scribe zone for isolating it for a chip is located in parts other than illustration of a wafer 10, it is drawing 1 (b). (c) The resin film 5 and a protective coat 4 are removed from this zone at a process.

[0014] Although up aperture 5a above required for a make lump of a bump electrode and lower aperture 4a end Since the direction of ** larger than lower aperture 4a has good up aperture 5a in case a ground film is put at the following process, at this example, it is drawing 1 (d). Drawing, up aperture 5a is extended to the side, as the resin film 5 is dissolved with an above-mentioned developer by using the photoresist film 30 as a mask at the shown up aperture spreading process and 5b shows. Since several micrometers or less of the amount of dissolutions of the resin film 5 in this case are sufficient, it should just carry out short-time being immersed of the wafer 10 at a developer. After this process end is about a wafer 10, after removing the photoresist film 30. The polyimide resin of the resin film 5 is completely stiffened by heating about 30 minutes to the temperature of 300 - 400 **. In addition, this up aperture spreading process is included and the photoresist film 30 is drawing 1 (b). It is used in the state [having attached to up aperture dawn processes]. Thus, by this invention method, up aperture 5a of the resin film 5 and lower aperture 4a of a protective coat 4 can be broken only in 1 time of the photograph process over the photoresist film 30, therefore the number of times of a photograph process can be decreased conventionally.

[0015] Drawing 1 (e) A bump electrode growth process is shown. This point is the same as the former. It is titanium etc. first. 0.2-0.5 PARAJUUMU equipped with covering of bottom ground film 6a of the thickness of mum, and about 0.02-micrometer very thin gold etc. 0.4-0.6 So that the ground film 6 which consists of top ground film 6b of the thickness of mum may be connected with the wiring film 3 by the spatter etc. After covering all over a wafer 10, patterning of the top ground film 6b is carried out to larger ** a little than up aperture 5a by photo etching. Next, the aperture in which the photoresist film 31 is attached to and only top ground film 6b is exposed according to a photograph process is broken, and gold is grown up into the bump electrodes 7 at a height of 10-20 micrometers with the alternative electrolysis plating which makes this the mask for plating and uses wrap bottom ground film 6a as a plating electrode for the whole surface of a wafer 10.

[0016] Drawing 1 (f) The completion state of the bump electrode 7 is shown. For that, it is drawing 1 (e). It is good by removing bottom ground film 6a from the front face of the resin film 5 by etching using the rare fluoric acid which uses top ground film 6b as a mask like usually, after removing the photoresist film 31 from a state first. Of course, a flip chip is isolated by carrying out the scribe of the wafer 10. Defects, such as a crack of a protective coat 4, are protected by the resin film 5 in the state of this completion, and the invasion of the open air is prevented. Moreover, since the

resin film 5 does not contact the wiring film 3 by this invention method so that an above-mentioned process may show, the front face is always kept pure and the bump electrode 7 is certainly connected very much with the wiring film 3 with low electric resistance through the ground film 6.
[0017]
[Effect of the Invention] After putting a protective coat first on the wiring film which should protrude a bump electrode as above according to this invention method, before hardening on it, a meltable resin film is applied with a developer. An up aperture is broken on a resin film with the developer for them at the same time it breaks the specification aperture of a bump electrode pattern on the photoresist film applied on this resin film. Subsequently, a lower aperture is broken in a protective coat by etching which uses a resin film as a mask, and the following effect can be raised by growing up the metal of a bump electrode alternatively with electrolysis plating on the wiring film exposed into the lower aperture.
[0018] (a) By applying a resin film, before breaking the aperture for bump electrodes in a wrap protective coat in the wiring film which should connect a bump electrode, and using a meltable thing with a developer, before hardening to this By breaking an up aperture on a resin film with the developer for them at the same time it breaks the aperture which specifies a bump electrode pattern to be a photoresist film, and breaking a lower aperture by etching which makes it a mask to a protective coat The need of adding a photograph process like before for a resin film can be abolished, the number of processes can be decreased, and manufacture of the flip chip for integrated circuit devices can be rationalized.
(b) Since a resin film does not contact a wiring film directly through all processes, while always keeping the front face of a wiring film pure, preventing generating of the faulty connection of the bump electrode by the residue of a resin film like before, its contamination, etc., and a wiring film and improving the manufacture yield of a flip chip, reliability can be raised together with the protective effect of the defect of the protective coat by the resin film over a long period of time [the]. Thus, this invention has the effect which reduces the manufacturing cost of the flip chip of a highly reliable integrated circuit device, improves the manufacture yield, and raises economical efficiency.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] The example of the manufacture method of the bump electrode by this invention is shown according to the state of the wafer for every main processes. This drawing (a) A protective coat covering process and a resin film application process, and this drawing (b) Up aperture dawn process, This drawing (c) A lower aperture dawn process and this drawing (d) An up aperture spreading process and this drawing (e) The important section expanded sectional view of the wafer in which the state of a bump electrode growth process is shown, respectively, and this drawing (f) It is the important section expanded sectional view of the wafer of a completion state.
[Drawing 2] It is the important section expanded sectional view of the conventional flip chip which is not equipped with a resin film.
[Drawing 3] The conventional method of making a bump electrode to flip chips equipped with a resin film is shown, and it is this drawing (a). A protective coat formation process and this drawing (b) A resin film application process and this drawing (c) The aperture dawn process to a resin film, and this drawing (d) It is the important section expanded sectional view showing the state of the flip chip of a bump electrode growth process.
[Description of Notations]
1 Semiconductor Substrate of Integrated Circuit Device
2 Insulator Layer
3 Wiring Film
4 Protective Coat
4a The lower aperture for bump electrodes
5 Resin Film
5a The up aperture for bump electrodes
6 Ground Film
6a Bottom ground film
6b Top ground film
7 Bump Electrode or Metal for Them

(19)日本国特許庁（ＪＰ）　(12)**公開特許公報（Ａ）**　(11)特許出願公開番号

特開平5－299421

(43)公開日　平成５年(1993)11月12日

(51)Int.Cl.[5]	識別記号	庁内整理番号	ＦＩ	技術表示箇所
Ｈ０１Ｌ　21/321				
		9168－4M	Ｈ０１Ｌ　21/ 92	Ｆ

審査請求　未請求　請求項の数３(全　５　頁)

(21)出願番号　特願平4－98382

(22)出願日　平成４年(1992)４月20日

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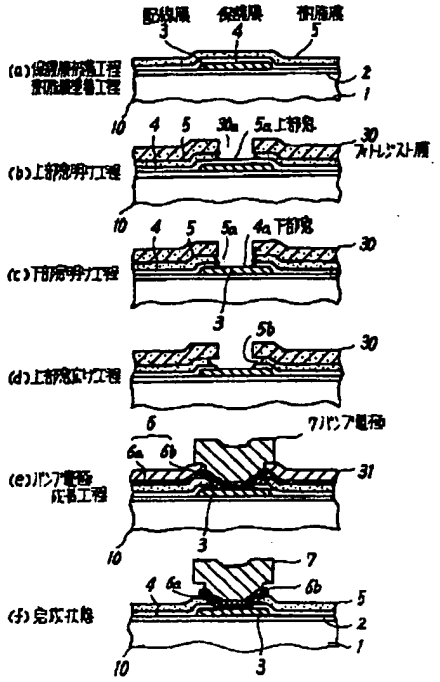
(54)【発明の名称】　集積回路装置用バンプ電極の製造方法

(57)【要約】

【目的】保護膜を樹脂膜で保護する集積回路装置のフリップチップに簡単な工程で歩留まりよくバンプ電極を作り込む。

【構成】バンプ電極７を突設すべき配線膜３の上に保護膜４を被着した後に樹脂膜５を塗着し、フォトレジスト膜30にバンプ電極のパターンを指定する窓を明けると同時にそれ用の現像液で樹脂膜５に上部窓5aを明け、樹脂膜５をマスクとするエッチングで保護膜４に下部窓4aを明けた後に、下部窓4aの中に露出する配線膜３と接続された下地膜６の上にバンプ電極７の金属を電解めっき法により成長させる。



1

【特許請求の範囲】

【請求項１】集積回路装置にその配線膜に接続されたバンプ電極を作り込む方法であって、配線膜上に保護膜を被着する工程と、保護膜上に硬化前に現像液により可溶な樹脂膜を塗着する工程と、樹脂膜上に塗着したフォトレジスト膜にバンプ電極パターンを指定する窓を明けると同時にそれ用の現像液により樹脂膜に上部窓を明ける工程と、この樹脂膜をマスクとするエッチングにより保護膜に下部窓を明ける工程と、下部窓の中に露出された配線膜の上にバンプ電極の金属を電解めっきにより選択的に成長させる工程とを含むことを特徴とする集積回路装置用バンプ電極の製造方法。

【請求項２】請求項１に記載の方法において、樹脂膜にポリイミド樹脂膜を用いることを特徴とする集積回路装置用バンプ電極の製造方法。

【請求項３】請求項１に記載の方法において、下部窓明け工程に続いて上部窓を側方に広げる工程を経た上でバンプ電極の成長工程を施すようにしたことを特徴とする集積回路装置用バンプ電極の製造方法。

【発明の詳細な説明】

【０００１】

【産業上の利用分野】本発明はチップ実装用の集積回路装置のフリップチップに外部接続用突起電極であるバンプ電極を作り込む方法に関する。

【０００２】

【従来の技術】外部接続用バンプ電極を備える上述のフリップチップは、パッケージ内に収納することなくそのままの形でチップ実装して実装のスペースと手間を大幅に節約できる特長があるため、最近では種々な電子装置への組み込み用に益々広く採用される傾向にあるが、使用中に熱サイクル等が掛かってチップの表面の保護膜にクラック等の欠陥が発生すると外気の侵入により特性の低下を招きやすい問題がある。以下、図２を参照してこの欠陥発生の様子を簡単に説明する。

【０００３】図２はフリップチップ20の要部拡大断面であり、集積回路が作り込まれたその半導体基板１の表面を覆う酸化シリコン等の絶縁膜２の上にアルミの配線膜３が配設されている。図の左側のチップ周縁部では、この配線膜３を覆う保護膜４に窓を明けてその中で配線膜３と接続するよう金，銅，はんだ等のバンプ電極７が薄い下地膜６を介して電解めっきによって突設される。下地膜６は通例のように電解めっき時にめっき電極として利用されるチタン等の下側下地膜6aと導電性の良好なパラジュウム等の上側下地膜6bの２層構成とされる。なお、実装の際にはフリップチップ20を図と逆に下に向けた姿勢でバンプ電極７を相手方と熱圧着やはんだ付けによって接合する。

【０００４】図の右側の中央部では、配線膜３が相互間に絶縁膜２を介しこの例では２層に配線されかつ保護膜４で覆われる。この保護膜４には窒化シリコン等の気密

2

性の高い無機絶縁材料が用いられ、膜質が緻密である反面硬くて張力が掛かると脆い欠点があり、図のように被覆段差の大きな個所に熱応力が集中してクラックＣが発生することがある。かかる欠陥が発生するとそこから外気，とくに水分が侵入して配線膜３のアルミを腐食させやすく、さらに半導体基板１の方にも侵入して集積回路の動作特性を低下させるおそれがある。

【０００５】このため、高信頼性を要するフリップチップでは従来から無機質の保護膜４を有機質の膜で保護している。この有機保護膜には強靭で耐熱性のよいポリイミド樹脂等が用いられる。図３にこの樹脂膜を備える場合のバンプ電極７を作り込む従来方法を示す。まず同図(a) のように保護膜４に窓4aを明けた後、同図(b) のように樹脂膜５用にポリイミド樹脂等をスピンコートして300～400 ℃の温度で充分に硬化させた上で、これに同図(c) のように窓5aをドライエッチング法等により明け、窓4aと5aの中に同図(d) のように上述の２層の下地膜６を介しバンプ電極７を電解めっきにより成長させる。なお、同図(b) の工程で樹脂膜５として感光性をもつポリイミド樹脂をスピンコートして、同図(c) の工程でそのフォトプロセスにより窓5aを明けた後に硬化させることもできる。

【０００６】

【発明が解決しようとする課題】上述のように無機質の保護膜４の上に有機質の樹脂膜５を重ねることにより、保護膜４にクラック等の欠陥が発生しても樹脂膜５により外気の侵入を防止してフリップチップ20の信頼性を大幅に高めることができるが、樹脂膜５を追加しただけ余分に手間が掛かるほかそれに付随して新たに問題が発生する。すなわち、フォトプロセスが従来の保護膜４のほかに樹脂膜５にも必要になるのでその分がコスト高になる。さらに、図３(b) の工程で配線膜３に付着した樹脂膜５を次の図３(c) の工程で完全に取り切れないことがあり、そのアルミ表面に樹脂膜５の残渣やそれによる汚染があるとバンプ電極７の接続不良が発生し製造歩留まりが低下する。本発明の目的は樹脂膜の追加によるかかるコスト高や歩留まり低下の問題を解決できるバンプ電極の製造方法を提供することにある。

【０００７】

【課題を解決するための手段】上述の目的は本発明方法によれば、バンプ電極を突設すべき配線膜の上にまず保護膜を被着した後その上に硬化前に現像液により可溶な樹脂膜を塗着し、この樹脂膜上に塗着したフォトレジスト膜にバンプ電極パターンの指定窓を明けると同時にそれ用の現像液によって樹脂膜に上部窓を明け、ついで樹脂膜をマスクとするエッチングにより保護膜に下部窓を明け、下部窓の中に露出された配線膜の上にバンプ電極の金属を従来と同じ要領で電解めっきにより選択的に成長させることによって達成される。

【０００８】本発明方法でも樹脂膜にポリイミド樹脂を

用いるのがよく、その溶解用現像液は有機アルカリ性，とくにアンモニア系のものが有利で、これに対応してフォトレジスト膜にポジ形を用いるのがよい。下部窓と上部窓からなるバンプ電極用の窓をそれに有利な上広がりの形状の縦断面に形成するには、保護膜の下部窓明け工程に引き続き現像液により樹脂膜の上部窓を側方に広げる工程をバンプ電極の成長工程の前に施すのが望ましい。なお、樹脂膜の加熱硬化はバンプ電極の成長工程に先立って行なうのがよい。

【０００９】

【作用】本発明方法は、従来と異なり配線膜を覆う保護膜にバンプ電極用の窓を明ける前に樹脂膜を塗着し、かつこれに硬化前に現像液により可溶なものを用いることにより、フォトレジスト膜にバンプ電極パターンを指定する窓を明けると同時にそれ用の現像液により樹脂膜に上部窓を明け、保護膜に対してはそれをマスクとするエッチングにより下部窓を明けることにより、従来のように樹脂膜のためにフォトプロセスを追加する必要をなくして工程数を減少させ、かつ全工程を通じ配線膜に樹脂膜が接触しないようにしてその汚染等によるバンプ電極と配線膜の接続不良の発生を防止するものである。

【００１０】

【実施例】図１を参照して本発明の実施例を説明する。バンプ電極は各フリップチップに単離する前のウエハに作り込まれ、本発明方法を構成する主な工程ごとの状態が同図(a) ～(f) にウエハ10の要部拡大断面で示され、図２以降に対応する部分に同じ符号が付けられている。図１(a) に示すようにバウエハ10の集積回路が作り込まれた半導体基板１の表面は酸化シリコンや燐シリケートガラスの絶縁膜２により 0.5～１μmの膜厚で覆われ、その上側に図示以外の個所で集積回路と接続された１μm程度の厚みのアルミの配線膜３が配設されている。

【００１１】図１(a) は保護膜被着工程と樹脂膜被着工程とを終了した状態を示す。保護膜被着工程では配線膜３の上を含むウエハ10の全面に窒化シリコン等の保護膜４を通例のようにプラズマＣＶＤ法等により例えば１μmの膜厚で被着する。従来はこの段階で図３(a) のように保護膜４に窓を明けていたが、本発明方法では窓を明けることなく引き続いて次の樹脂膜被着工程でその上に樹脂膜５を塗着する。この樹脂膜５には硬化後に強靭な強度を有しかつ耐熱性が高いポリイミド樹脂を用いるのがよく、溶剤で適宜な粘度に希釈したその樹脂液を２～３μmの膜厚でウエハ10の全面にスピンコートし、かつこの樹脂膜塗着工程では溶剤だけを蒸発させて未硬化で従って現像液に可溶な状態に留めて置く。

【００１２】図１(b) に上部窓明け工程を示す。この工程ではまずウエハ10の全面にフォトレジスト膜30をスピンコートし、これにフォトプロセスでふつうは数十μm径や角であるバンプ電極のパターンを焼き付けた上、現像液によってそれに窓30ａを抜くと同時に同じ現像液で樹脂膜５を溶解させて上部窓5aを明ける。かかる同時窓明け用の現像液にはアンモニア系の有機アルカリ（例えばAZ303）を用いるのがよく、これに対応してフォトレジスト膜30にポジ形を用いるのがよい。

【００１３】図１(c) に下部窓明け工程を示す。この工程では上部窓5aを備える樹脂膜５をマスクとするエッチングにより保護膜４に下部窓4aを明けて配線膜３のアルミを露出させる。この窓明けエッチングには通例のように５～10%のO_2を含む CF_4を反応ガスとするドライエッチングを利用することでよいが、この際に保護膜４の下部窓4aが樹脂膜５の上部窓5aより若干広くなるまでオーバエッチングを施して配線膜３の表面を充分に清浄化するのが望ましい。なお、ウエハ10の図示以外の個所にそれをチップに単離するためのスクライブゾーンがあるので、図１(b) と(c) の工程でこのゾーンから樹脂膜５と保護膜４が除去される。

【００１４】以上でバンプ電極の作り込みに必要な上部窓5aと下部窓4aとが明けられるが、次工程で下地膜を被着する際に上部窓5aが下部窓4aより広いめの方がよいので、この実施例では図１(d) に示す上部窓広げ工程でフォトレジスト膜30をマスクとして上述の現像液により樹脂膜５を溶解して上部窓5aを図で5bで示すよう側方に広げる。この際の樹脂膜５の溶解量は数μm以下でよいのでウエハ10を現像液に短時間浸漬するだけでよい。この工程終了後は、フォトレジスト膜30を除去した上でウエハ10を 300～400 ℃の温度に30分程度加熱することによって樹脂膜５のポリイミド樹脂を完全に硬化させる。なお、この上部窓広げ工程を含めてフォトレジスト膜30は図１(b) の上部窓明け工程用に付けたままの状態で利用される。このように、本発明方法ではフォトレジスト膜30に対する１回のフォトプロセスだけで樹脂膜５の上部窓5aと保護膜４の下部窓4aとを明けることができ、従って従来よりフォトプロセス回数を減少させることができる。

【００１５】図１(e) にバンプ電極成長工程を示す。この要領は従来と同じであって、まずチタン等の 0.2～0.5 μmの膜厚の下側下地膜6aと0.02μm程度のごく薄い金の被覆を備えるパラジュウム等の 0.4～0.6 μmの膜厚の上側下地膜6bとからなる下地膜６を配線膜３と接続するようにスパッタ法等によりウエハ10の全面に被着した上で、フォトエッチングにより上側下地膜6bを上部窓5aより若干大きいめにパターンニングする。次に、フォトレジスト膜31を付けてフォトプロセスにより上側下地膜6bのみを露出させる窓を明け、これをめっき用マスクとしウエハ10の全面を覆う下側下地膜6aをめっき電極とする選択的な電解めっきによってバンプ電極７用に例えば金を10～20μmの高さに成長させる。

【００１６】図１(f) にバンプ電極７の完成状態を示す。このためには図１(e) の状態からまずフォトレジスト膜31を除去した上で、通例のように上側下地膜6bをマ

スクとする希ふっ酸等を用いるエッチングによって下側下地膜6aを樹脂膜５の表面から除去することでよい。もちろん、ウエハ10をスクライブすることによりフリップチップが単離される。この完成状態では樹脂膜５により保護膜４のクラック等の欠陥が保護されて外気の侵入が防止される。また、上述の工程からわかるように本発明方法では配線膜３に樹脂膜５が接触することがないので、その表面が常に清浄に保たれてバンプ電極７が下地膜６を介してごく低い電気抵抗で配線膜３と確実に接続される。

【００１７】

【発明の効果】以上のとおり本発明方法によれば、バンプ電極を突設すべき配線膜の上にまず保護膜を被着した後その上に硬化前に現像液により可溶な樹脂膜を塗着し、この樹脂膜上に塗着したフォトレジスト膜にバンプ電極パターンの指定窓を明けると同時にそれ用の現像液によって樹脂膜に上部窓を明け、ついで樹脂膜をマスクとするエッチングにより保護膜に下部窓を明け、下部窓の中に露出された配線膜の上にバンプ電極の金属を電解めっきにより選択的に成長させることにより、次の効果を上げることができる。

【００１８】(a) バンプ電極を接続すべき配線膜を覆う保護膜にバンプ電極用の窓を明ける前に樹脂膜を塗着し、かつこれに硬化前に現像液により可溶なものを用いることにより、フォトレジスト膜にバンプ電極パターンを指定する窓を明けると同時にそれ用の現像液により樹脂膜に上部窓を明け、保護膜に対してはそれをマスクとするエッチングにより下部窓を明けることにより、従来のように樹脂膜のためにフォトプロセスを追加する必要をなくして工程数を減少させ、集積回路装置用のフリップチップの製造を合理化することができる。

(b) 全工程を通じて配線膜に樹脂膜が直接に接触することがないので配線膜の表面を常に清浄に保って、従来のような樹脂膜の残渣やその汚染等によるバンプ電極と配線膜の接続不良の発生を防止してフリップチップの製造歩留まりを向上するとともに、樹脂膜による保護膜の欠陥の保護効果と合わせてその長期信頼性を高めることができる。

このように本発明は高信頼性の集積回路装置のフリップチップの製造コストを低減し製造歩留まりを向上して経済性を高める効果を有する。

【図面の簡単な説明】

【図１】本発明によるバンプ電極の製造方法の実施例を主な工程ごとのウエハの状態により示し、同図(a) は保護膜被着工程および樹脂膜塗着工程、同図(b) は上部窓明け工程、同図(c) は下部窓明け工程、同図(d) は上部窓広げ工程、同図(e) はバンプ電極成長工程の状態をそれぞれ示すウエハの要部拡大断面図、同図(f) は完成状態のウエハの要部拡大断面図である。

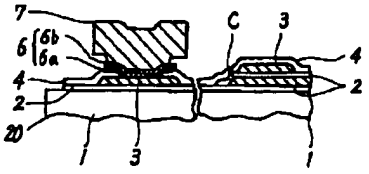
【図２】樹脂膜を備えない従来のフリップチップの要部拡大断面図である。

【図３】樹脂膜を備えるフリップチップ用にバンプ電極を作り込む従来の方法を示し、同図(a) は保護膜形成工程、同図(b) は樹脂膜塗着工程、同図(c) は樹脂膜への窓明け工程、同図(d) はバンプ電極成長工程のフリップチップの状態を示す要部拡大断面図である。

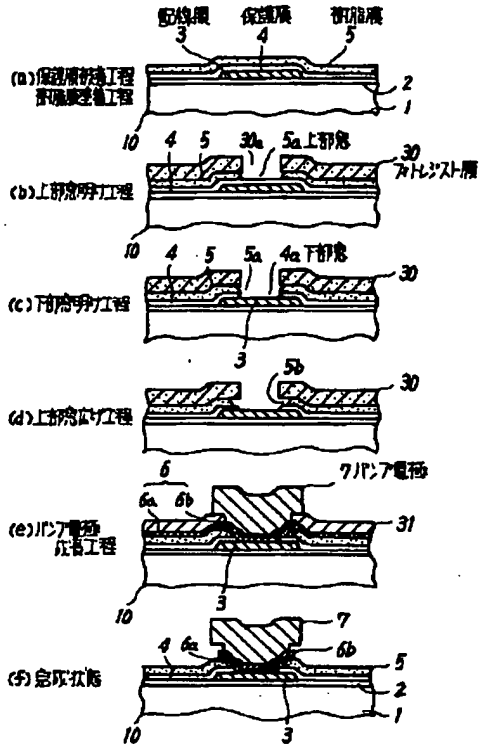
【符号の説明】

1	集積回路装置の半導体基板
2	絶縁膜
3	配線膜
4	保護膜
4a	バンプ電極用の下部窓
5	樹脂膜
5a	バンプ電極用の上部窓
6	下地膜
6a	下側下地膜
6b	上側下地膜
7	バンプ電極ないしはそれ用の金属

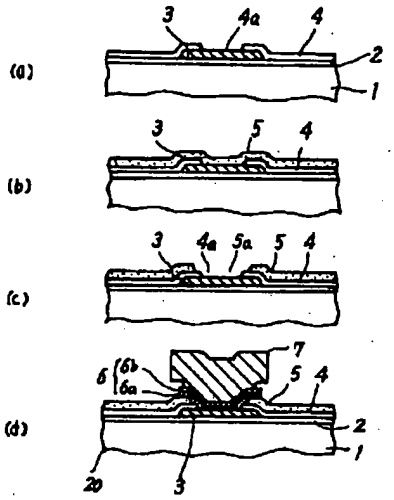
【図２】



【図１】


配線層
保護膜
開口部
3
4
5
(a)保護膜形成工程
開口部形成工程
2
1
10
4
5
30a
5a 上部窓
30
アパレジスト層
(b)上部窓明け工程
5a
4a 下部窓
(c)下部窓明け工程
5b
(d)上部窓広げ工程
6
7 バンプ電極
6a
6b
31
(e)バンプ電極
位置工程
(f)金属拡散

【図３】


(a)
3
4a
4
2
1
(b)
5
(c)
(d)
7
6
6b
6a
20